# INTEGRATED CIRCUIT AND ASSOCIATED DESIGN METHOD USING SPARE GATE ISLANDS

## ABSTRACT

An integrated circuit includes standard cells interspersed with islands of spare gates. The spare gates are arranged in multiple groups of spare gates, with each group of spare gates within a corresponding designated spare gate area of a standard cell portion of the integrated circuit. At least a given one of the groups of spare gates is arranged between first and second rows of the standard cells and includes one or more rows of spare gates, with each row of spare gates including multiple base transistor structures arranged adjacent to one another along longitudinal dimensions of the structures. The standard cells and spare gates are preferably placed in accordance with a placement operation of an automated place and route process of a standard cell computer-aided design (CAD) tool. The spare gates may be implemented using a base transistor structure compatible with the standard cell CAD tool. The spare gate islands may be distributed throughout the standard cell portion of the integrated circuit in a substantially uniform manner, for example, in accordance with a predetermined geometric pattern. The spare gates may be converted to active gates in conjunction with the automated place and route process using only conductors in one or more metal layers of the integrated circuit.